**Career objective**

To instil the younger generation with positive energy and a never ending hunger towards gaining knowledge and increase my own depth in my areas of interest and learn more of the unexplored parts of the study, in an institute offering new challenges and opportunities to further cone my abilities and push myself towards achieving excellence and sharing my knowledge through their medium.

**Education**

08/2015-present **Master of Technology**

 Specialization: Power system and control

 University: National Institute of Technology, Raipur

 Master’s thesis: “Development of novel fault tolerant multi-level inverter topology”

 Study emphasis: Reduced count device in power converter topology with fault tolerant

 characteristics and capacitor voltage balancing

 Grade: 7.61 CPI

07/2009-06/2013 **Bachelor of Technology**

 Specialization: Electrical and electronics engineering

 University: Uttarakhand technical university, Uttarakhand

Bachelor’s project: “Image compression and facial recognition”

 Study thesis: Extracting the data from the captured image and comparing with

 the database images

Percentage: 64.35%

07/2008-04/2009 **Intermediate**

 Specialization: Physics, Chemistry and Mathematics

 University: Central Board of Secondary Education

 Percentage: 73%

06/2006-04/2007 **Matriculation**

 University: Indian Certificate for Secondary education

 Percentage: 88%

**Publication(s)**

1. Paper titled, “A single phase fault tolerant multi-level inverter topology”, accepted in IEEE international conference on Recent Trends in Electronics, Information and Communication Technology (IRTEICT) in Bangalore, India on 19-20th May, 2017.

2. Paper titled, “Single and multi-switch fault tolerant topology of multi-level inverter”, submitted in IEEE International Conference on Industrial Electronics Control and Instrumentation (IECON), 2017, China

**Fellowship**

Prestigious recipient of GATE (Graduate Aptitude Technical Examination) qualified fellowship awarded by MHRD (Ministry of Human Resource Development) during my post-graduation

**Skill set**

* Matlab, PowerSim
* A six week training in PLC (Programmable Logic Controller) and SCADA (Supervisory Control and Data Acquisition)

**Examinations and Paper qualified**

* Qualified GATE (Graduate Aptitude Technical Examination) 2014, 2015 with AIR 2727 and 3522 respectively
* Achieved 88 percentile in CAT, 2014 (Common Aptitude Test)
* Qualified Elitmus paper
* Qualified AMCAT paper

**Languages**

* English, Hindi, Punjabi, Italian (Beginner)

**References**

1. Dr. Lalit Kumar, Department of electrical engineering, National Institute of technology, Raipur

 lkumar.ele@nitrr.ac.in

2. Dr. S. Ghosh, Department of electrical engineering, National Institute of technology, Raipur

 sgosh.ele@nitrr.ac.in

Date: July 4, 2017 (Manik Jalhotra)

Place: Raipur